Statement of Volatility – Dell PowerEdge R930

Dell PowerEdge R930 contains both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge R930 server.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
Planer				
PBG Internal CMOS NVRAM	Non-Volatile	1	U_PBG	256 Bytes
BIOS SPI Flash	Non-Volatile	1	U_SPI_BIOS	16MB
iDRAC SPI Flash	Non-Volatile	1	U_IDRAC_SPI	4MB
IDRAC SDRAM	Volatile	1	U_IDRAC_MEM	2Gb
BMC EMMC	Non-Volatile	1	U_EMMC	4GB
CPU Vcore and VSA Regulators	Non-Volatile	4	EU_CPU1_VR,EU_CPU2_VR, EU_CPU3_VR,EU_CPU4_VR	4.25KB
System CPLD	Non-Volatile	2	U_CPLD1, U_CPLD2	8Kb (1700 microcell's)
TPM	Non-Volatile	1	U_TPM	128 Bytes
Power Supplies				
PSU FW	Non-Volatile	1 per PSU	Varies by part number	Up to 2MB Varies by part number
24x2.5" SAS Backplane				
BP FRU image	Non-Volatile	1	U_BP_FRU	2Kb

16+8x2.5" PCIe SSD Backplane				
SEP internal flash	Non-Volatile	2	U_SEP1 U_SEP2	Flash: 32KB + 4KB EEPROM: 1KB SRAM: 4KB
4x2.5" 12GB Backplane				
SEP internal flash	Non-Volatile	1	U_SEP	Flash: 32KB + 4KB EEPROM: 1KB SRAM: 4KB
Active I/O Riser Right				
FRU	Non-Volatile	1	U_IORR_FRU	2Kb
Configuration EEPROM	Non-Volatile	1	U_IOR_SPI	256Kb
Active I/O Riser Left				
FRU	Non-Volatile	1	U_IORL_FRU	2Kb
Configuration EEPROM	Non-Volatile	1	U_IOR_SPI	256Kb
12GB Daughter Card (Performance or Unified)				
Expander Flash memory	Non-Volatile	1	U_EXP_FLASH	128Mb
Expander NVSRAM	Non-Volatile	1	U_EXP_NVRAM	1Mb
Expander FRU image	Non-Volatile	1	U_EXP_EEPROM	2Kb
Memory Riser				
Mem FRU image	Non-Volatile	1	U_MEM_FRU	2Kb
MEM VDDQ Regulators	Non-Volatile	2	U_MEM_VRAB; U_MEM_VRCD	4.25KB
System Memory	Volatile	Up to 24 per CPU	CPU<4:1>_CH<3:0>_D<2:0> per Riser/ 2 Risers per CPU	Up to 32GB per DIMM

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
Planer			
PBG Internal CMOS NVRAM	Battery-backed CMOS NVRAM	No	Real-time clock and BIOS configuration settings
BIOS SPI Flash	SPI Flash	No	Boot code, system configuration information, UEFI environment, Flash Disceptor, ME
iDRAC SPI Flash	SPI Flash	No	iDRAC Uboot (bootloader), server management persistent store (i.e. IDRAC MAC Address, iDRAC boot variables), lifecycle log cache, virtual planar FRU and EPPID, rac log, System Event Log, JobStore, iDRAC Secure Boot Code,
IDRAC SDRAM	IDRAC SDRAM	No	Video memory written by IDRAC memory interface.
BMC EMMC	eMMC NAND Flash	No	Operational iDRAC FW, Lifecycle Controller USC partition, LC service diag., LC OS drivers, USC firmware
CPU Vcore and VSA Regulators	OTP(one time programmable)	No	Operational parameters
System CPLD	CPLD	No	Operational parameters and system control.
TPM	EEPROM	No	Stores encryption keys for TPM functionality
Power Supplies			
PSU FW	Embedded microcontroller flash	No	Power Supply operation, power management data and fault behaviors
24x2.5" SAS Backplane			
BP FRU image	I2C EEPROM	No	FRU
16+8x2.5" PCIe SSD Backplane			
SEP internal flash	Integrated Flash+EEPROM	No	Firmware + FRU
4x2.5" 12GB Backplane			
SEP internal flash	Integrated Flash+EEPROM	No	Firmware + FRU

Active I/O Risers			
I/O Riser FRU image	I2C EEPROM	No	FRU
Configuration image	EEPROM	No	Firmware that configures PEX switch ports and feature support
12GB Daughter Card (Performance or Unified)			
Flash memory	Flash	No	Firmware
Expander NVRAM	NVRAM	No	Expander Logging Storage during run time
Expander FRU image	I2C EEPROM	No	FRU
Memory Riser			
Mem FRU image	I2C EEPROM	No	FRU
MEM VDDQ Regulators	OTP(one time programmable)	No	Operational parameters
System Memory	RAM	Yes	System OS RAM

Item	How is data input to this memory?	How is this memory write protected?
Planer		
PBG Internal CMOS NVRAM	BIOS	N/A – BIOS only control
BIOS SPI Flash	SPI interface via iDRAC	Software write protected
iDRAC SPI Flash	SPI interface via iDRAC	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.
IDRAC SDRAM	Video Interface	N/A – Embedded iDRAC video subsystem only
BMC EMMC	NAND Flash interface via iDRAC	Embedded FW write protected
CPU Vcore and VSA Regulators	Once values are loaded into register space a cmd writes to nvram.	There are passwords for different sections of the register space
System CPLD	OTP(one time programmable) at factory	N/A – Factory only control
TPM	Data is pre-programmed by vendor. Keys are updated using TPM-enabled operating systems.	Software write protected
Power Supplies		

PSU FW	Different vendors have different utilities and tools to load the data to memory. It can also be loaded by Dell Update Package from LC or OS (Windows and Linux)	Protected by the embedded microcontroller. Special keys are used by special vendor provided utilities to unlock the ROM with various CRC checks during load.
24x2.5" SAS Backplane		
SEP internal flash	I2C interface via iDRAC	Program write protect bit
16+8x2.5" PCIe SSD Backplane		
SEP internal flash	I2C interface via iDRAC	Program write protect bit
4x2.5" 12GB Backplane		
SEP internal flash	I2C interface via iDRAC	Program write protect bit
Active I/O Risers		
FRU	Pre-programmed at manufacturing	No write protection
Configuration image	Pre-programmed at manufacturing	Protected by switch controller which special tool or application can be used for programming
12GB Daughter Card (Performance or Unified)		
Flash memory	Common Flash memory Interface (CFI)	Hardware strapping
Expander NVRAM	Written by Expander FW	Software write protected
Expander FRU image	I2C interface via iDRAC	Hardware strapping
Memory Riser		
Mem FRU image	I2C interface via iDRAC	FRU is not write protected
MEM VDDQ Regulators	Once values are loaded into register space a cmd writes to nvram.	There are passwords for different sections of the register space
System Memory	System OS	OS Control

NOTE: For any information that you may need, direct your questions to your Dell Marketing contact.